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Use of the "Via-In-Pad" Method to Ensure the High-Density Layout of the Conductive Pattern when Designing Multilayer Switching Structures

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Abstract **— The application features of the Via-in-Pad method when implementing a high-density conductive pattern of multilayer switching structures in electronics is considered herein. The composition method for vias and contact pads for the tracing ability improvement is proposed, and the assessment methodology for the effective area utilization for BGA components is presented. The experimental study of the pressure sensor housing was carried out, which showed that the application of this method made it possible to reduce the number of vias by 40% and place more contact pads per unit area, which frees up the gaps for BGA tracing, reduces the pattern density and microwave signal paths. The obtained results confirmed the possibility of reduction of the usable space by 25%, which makes it possible to arrange more pads per unit area, to free up the gaps for BGA tracing, to reduce the time for drilling the workpieces, to reduce the number of used drills, and also provides the best heat removal from the components. The disadvantage is the large internal resistance of the transitions created by the Via-in-Pad method, in contrast to the standard ones, which can negatively affect the flow of critical signals. By comparing the resistances from the metallization layer of the via in the MPCB with a flexible flat cable and in the MPCB designed using the Via-in-Pad method, it was found that the Via-in-Pad method made it possible to increase the layout efficiency of multilayer printed circuit boards.**

Keywords— **printed circuit board; BGA; SMD; tracing; thermal expansion coefficient (TEC); metallization; conductive material.**

I. INTRODUCTION

Current trends in the development of technological methods for designing multilayer printed circuit boards are characterized by an increase in the level of integration of the components on the functional nodes of electronic equipment and a decrease in the coordinate grid of switching structures [1]. The possibilities of minimizing the layout for via mounted components (VMCs) and surface mounted components (SMCs) are almost exhausted. Therefore, it can be stated that the limits for increasing the level of such integration are currently reached. This provision determines the relevance of this study because it presents ways to further solve the problem of integration of the components on functional units of electronics, which are found in the field of the spatial layout of the elements of functional nodes (3DMID) and metallization technology for vias of the multilayer printed circuit boards (MPCBs) [2], [3].

The above-mentioned provisions make it possible to formulate the purpose of the study, which is to find new solutions to reduce or eliminate the distances in vias of multilayer printed circuit boards. One of the most interesting approaches is to form vias of multilayer printed circuit boards inside the contact pads, the so-called "Via-in-Pads" (hole in the contact pad). In this case, vias should be filled with special pastes, both conductive and non-conductive. This technology aims at solving the problem of reduction of the area occupied by vias between the layers of the switching structure [4]-[10]. Let us consider in more detail the mechanism of this approach and its effectiveness.

II. MATERIAL AND METHOD

Switching structures, that is, specially formed conductive media, designed for switching and transmitting the signals between various modules and submodules of electronic equipment (EE), are the basis of the functional units of modern EE. Switching structures are used at all levels of electronic modules: connections inside the integrated circuits (metallization), connections between different electronic products (printed circuit boards), connections between electronic equipment units (cables, loops), etc. Switching structures for EE must have minimum active and inductive

resistance, the wave impedance, uniform over the length of the structure, minimum electromagnetic field around the line when current flows along with it, the ability to transmit signals in a wide range of frequencies, currents, and voltages. It is impossible to satisfy all of the above requirements using any one type of switching structure (SS). Therefore, various types of SSs are used depending on the functional features of both the SSs themselves and the equipment. The choice of the constructive-technological variant of the execution of the joints is an important and difficult task, which significantly affects the quality of the designed equipment. Moreover, in the conditions of complementarity, product characteristics determine the formation of cooperation networks [11]. Figure 1 shows the geometric parameters of some types of switching structures [1].

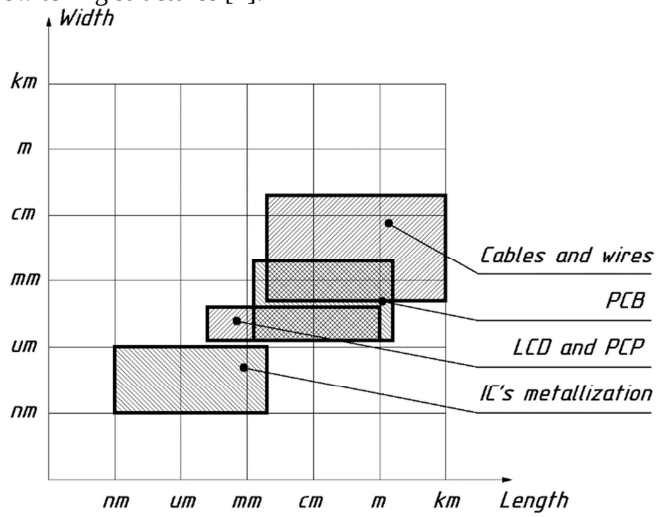


Fig. 1. The geometric parameters of some types of switching structures

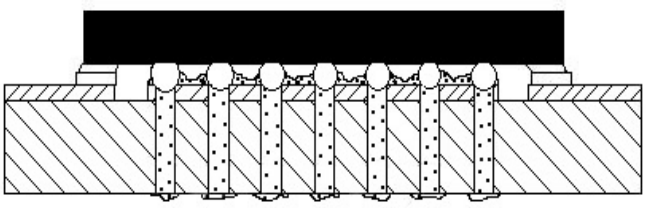
Currently, the increasing complexity of electronic equipment and its miniaturization lead to a shift in the geometric dimensions of switching structures in the micro- and nano-area [12]-[14]. The reduction of the size of electrical connections reduces the attenuation and signal distortion. The reduction of the width of printed conductors makes it possible to increase the density of installation and the accuracy of the manufacture of printed circuit boards.

The implementation of SSs in the form of one-sided (OSPCB) or double-sided printed-circuit boards (DSPCB) did not require a high density of the layout, which allowed the use of conventional through metallization. The main purpose of the PCB metallization process is to obtain conductive sections of the PCB (conductors, metalized vias, pads, terminal connectors, lamellas, etc.). Also, the PCB metalization can protect them from pickling during copper pickling operations from whitespace and from oxidation to ensure PCB solderability [1].

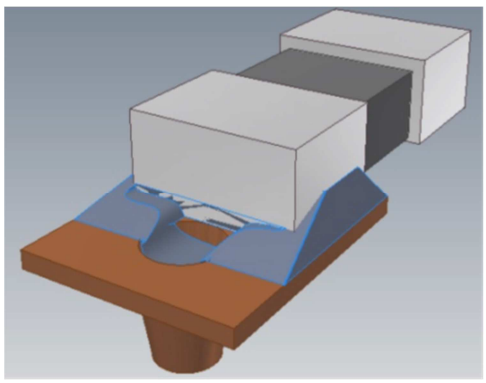
Via metallization processes are an integral part of PCB production, and the reliability of products depends, to a large extent on their quality. Long-term reliability is determined largely by the quality and uniformity of copper deposited in the hole. In this case, the metallization process preceding the deposition of galvanic copper is a critical factor in the successful deposition of a uniform copper layer in a through or blind hole. It is the process of the so-called preliminary metallization, in which a thin conductive layer is formed in the holes, that determines the continuity of the galvanic copper and the adhesion of the metallization column to the walls of the holes. To obtain a thin conductive layer, a chemical copper plating process or a “direct metallization” process can be used. Each of these processes has its own characteristics [15], [16]. Analyzing the metallization methods, one can distinguish [4]: chemical metallization; galvanic metallization; magnetron, ion-plasma and other spraying methods.

Over time, SSs became increasingly complex and required greater accuracy and the requirements for the area occupied by components and tracing toughened. Multilayer printed MPCBs appeared [1]. It is known that the transition hole of the printed circuit board is an opening in the printed circuit board with a conductive material on its wall, designed to electrically connect the conductive patterns of the PCB located on different conductive layers of the PCB. In the case of MPCBs, vias are of three types [1]: *through-holes; blind vias; buried vias*. This paper considers mainly through-holes, which make it possible to connect any BGA/SMD components to the inner layers [26]-[29].

When Via-in-Pads are used inside the pads, any soldering causes the penetration of the solder (solder paste) into the via. In the specific case of BGA components, the penetration of the solder causes the destruction of the output ball leads, as shown in Figure 2. Also, when soldering, the air in the hole can enter the solder joint, reducing its reliability to a critical level [17].



a) view 2D



b) view 3D

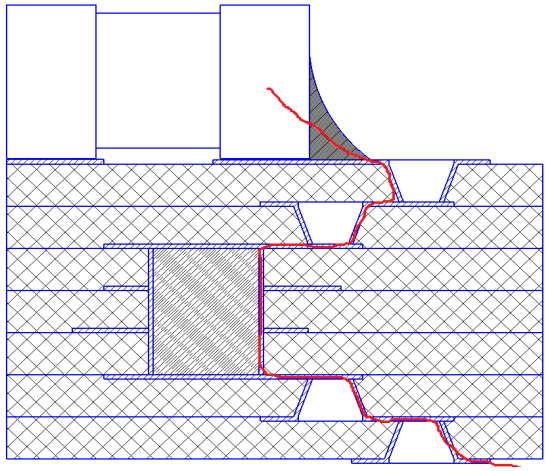
Fig. 2. Penetration of the solder into the through-holes of the DSPCB

This defect results in a deterioration in the electrical properties of the BGA with the board. Therefore, penetration into the holes and deterioration of the mechanical properties of the component must be prevented. The solution to this problem is the use of special conductive/non-conductive pastes with plating holes. Currently, vias are filled with polymeric materials. The use of polymers for these purposes

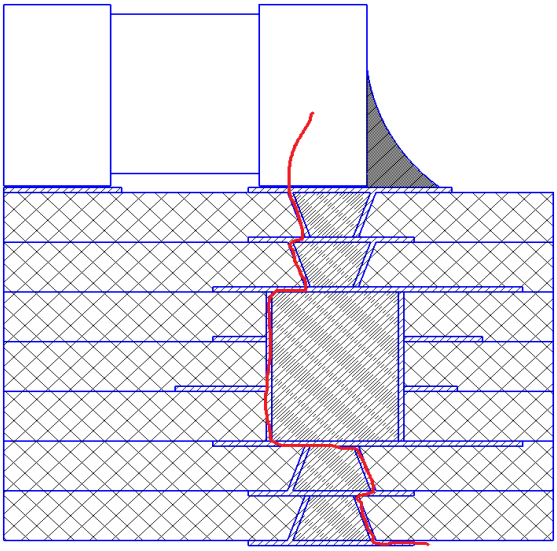
is increasingly expanding; the materials and the processes necessary for this are increasingly improved [18].

The researchers suggested that the arrangement of the vias inside the pads can increase the tracing ability and efficiency of utilization of the useful area of the PCB, as well as provide the possibility to use fewer layers. This is called the Via-in-Pad method.

Figure 3 shows the Via-in-Pad method in the context, where the reduction of the signal path is clearly shown, and one can also see the release of the area, for example, under a through-hole or under any other operations with a PCB [7].



a) MPCB with gaps for vias



b) MPCB with the Via-in-Pad method

Fig. 3. Via-in-Pad sectional view

With the help of the Via-in-Pad method, a number of problems are partially or completely solved: the release of the area for through-holes; the reduction of the route (for example, for RAM); the facilitation of the process of MPCB creation (using the method of sequential layer building); an increase in the tracing ability and efficiency of use of the area; MPCB wiring becomes intuitively easier in any program.

However, at the moment, there are some unresolved problems related to the combination of the contact pad and the vias, which is important to increase the tracing ability. Based on the conducted review, the authors offer new possibilities for using the Via-in-Pad method, which will solve the above problems [7].

III. Results and Discussion

To substantiate the main advantage of the application of the Via-in-Pad method, a technique has been developed, based on the calculation of the cleared area for tracing conductors using an example of a typical site for a BGA component (Figure 4). In standard tracing, the vias are arranged at equal distance from the pads of the BGA component, that is, at a distance equal to $\frac{\sqrt{2}}{2}g$. The dimensions d_{PAD}, d_{VIA} and l are selected by the designer of the circuit board. The size of g is specified by the component manufacturer. All these values are initial for further calculation.

The calculation is made for two cases: definition of the area with the minimum and maximum dimensions of the connecting track.First, the formulas for the calculation of the area are substantiated.

The areas of pads (PAD) and vias (VIA) are calculated using the circumference formula (Figure 4):

$$S_{PAD} = \pi \frac{d_{PAD}^{\ 2}}{4}, \quad (1)$$

$$S_{VIA} = \pi \frac{d_{VIA}^{\ 2}}{4}. \quad (2)$$

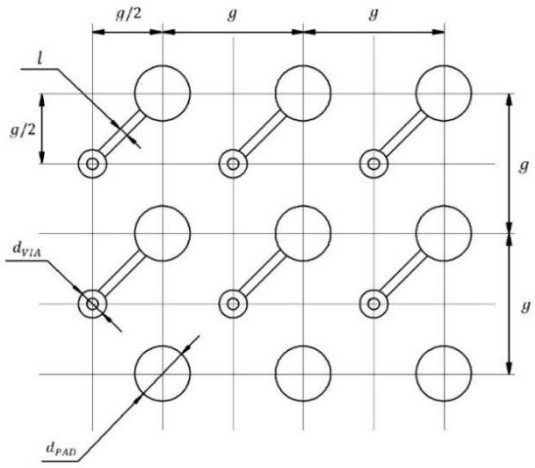


Fig. 4. Typical site for a BGA component with vias (Via) for pads (Pad): g – output step; d_{VIA} – diameter of the via; d_{PAD} – diameter of the pad; l – thickness of the connection line between the via and the pad

The area of the connecting track with $l < d_{VIA}$ and $l = d_{VIA}$ is calculated by the formulas (3) and (4) respectively (Figure 5, respectively):

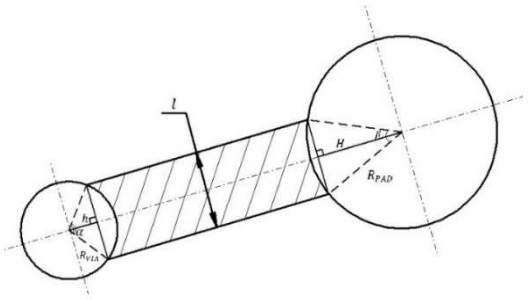
$$S_{CON} = l\left(\frac{\sqrt{2}}{2}g - h - H\right) - \frac{d_{VIA}^{\ 2}}{4}\left(\pi\frac{\alpha}{180^\circ} - \sin\alpha\right) - \quad (3)$$

$$- \frac{d_{PAD}^{\ 2}}{4}\left(\pi\frac{\beta}{180^\circ} - \sin\beta\right),$$

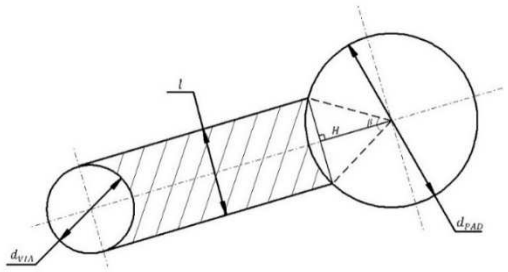
where $h = \sqrt{\frac{d_{VIA}^2}{4} - \frac{d_{VIA}^2}{16}} = \sqrt{\frac{3d_{VIA}^2}{16}}$ is the distance to the chord in the via; $H = \sqrt{\frac{3d_{PAD}^2}{16}}$ is the distance to the chord in the pad;

$\beta = 180^\circ - 2\arccos(\frac{l}{d_{PAD}})$; $\alpha = 180^\circ - 2\arccos(\frac{l}{d_{VIA}})$.

$$S_{CON\,max} = l\left(\frac{\sqrt{2}}{2}g - H\right) - \frac{d_{PAD}^2}{4}\left(\pi\frac{\beta}{180^\circ} - \sin\beta\right) - \frac{S_{VIA}}{2}. \quad (4)$$



a) with $l < d_{VIA}$



b) with $l = d_{VIA}$

Fig. 5. Connecting track area

The area of the contact pad zone is generally assumed to be equal to g^2. Then the free space of the area is calculated for three cases: with a via and a connecting track of minimum dimensions (5), with a via and a connecting track of maximum dimensions (6) and with a via in the contact pad (7):

$$S_{Z\,min} = g^2 - (S_{PAD} + S_{VIA} + S_{CON\,min}), \quad (5)$$

$$S_{Z\,max} = g^2 - (S_{PAD} + S_{VIA} + S_{CON\,max}), \quad (6)$$

$$S_{ZF} = g^2 - S_{PAD}. \quad (7)$$

The ratio of the occupied space in the zone of the contact pad to the area of the zone of the contact pad is expressed as a percentage.

$$F_{Z\,min} = \frac{S_{Z\,min}}{g^2} \cdot 100\%, \quad (8)$$

$$F_{Z\,min} = \frac{S_{Z\,max}}{g^2} \cdot 100\%, \quad (9)$$

$$F_{Z\,min} = \frac{S_{ZF}}{g^2} \cdot 100\%. \quad (10)$$

The result of the calculation is the range: $(F_{Z\,min} - F_{ZF}\ ; F_{Z\,max} - F_{ZF})$.

The calculation algorithm (Figure 7) and the corresponding listing are presented in Appendix.

The developed algorithm is implemented as the application software BGA-VIA-IN-PAD Analyzer (C++) (Appendix).

To check the operation of the algorithm and obtain the results, the following typical parameters are used: g = 1.27 mm; d_{VIA} = 0.6 mm; d_{PAD} – 0.8 mm; l = 0.4 mm. Based on the calculation results, the following values are obtained: (20.4-25.4)%. That is, up to 25% of the space for tracing can be freed using the Via-in-Pad method.

In the framework of the study, the MPCB of the signal processing module was analyzed using an example of a strain gauge.

REC Nanotechnological Systems and Nanoelectronics (REC Nanosystems) of the Department "Design and Production Technology of Electronic Equipment" of N.E. Bauman MSTU produces a model line of pressure sensors, for example, strain gauge SEAZh.406233.001 (Figure 6) [19, 20]. Brief specifications of this sensor are the following: operating pressure from 0.1 to 10 MPa, temperature range from + 60 to +185 °C, non-linearity minimum 0.1%.

The sensor provides continuous uniform over the range conversion of pressure into a unified analog signal.

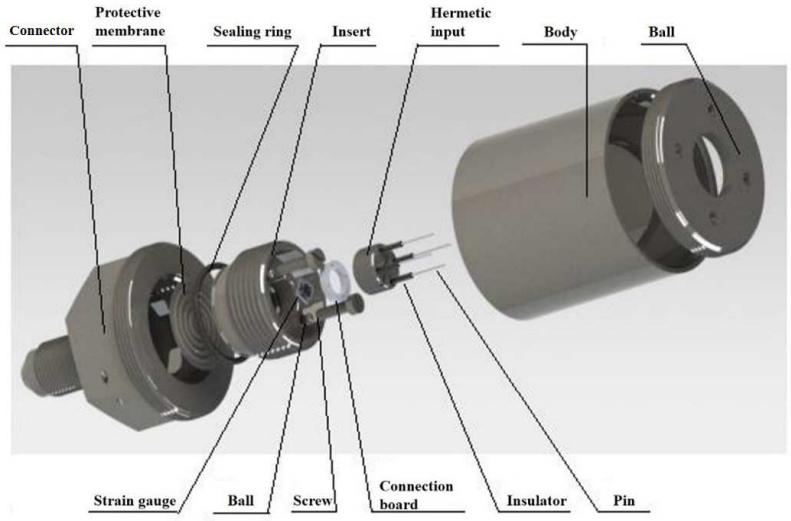


Fig. 6. Composition of the pressure sensor SEAZh.406233.001

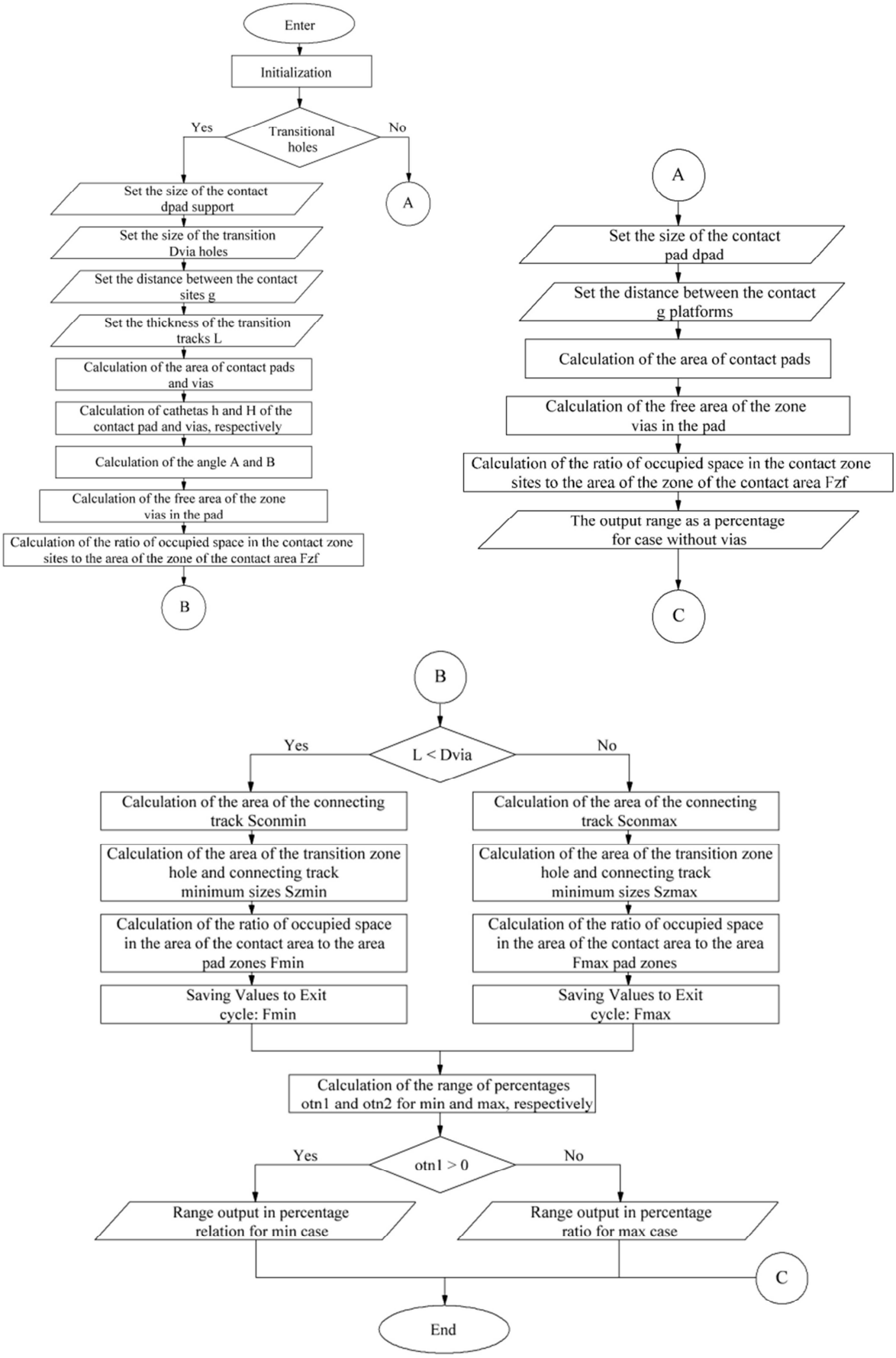


Fig. 7. Efficiency evaluation algorithm for the Via-in-Pad method

In general, the pressure sensor is connected to the measuring channel using a structural element for supplying pressure, through which pressure is supplied to the pressure transducer. For cylindrical sensors, for example, SEAZh.406233.001, the pre-processing and signal transmission module is located inside the sensor housing, and the housing must be radio transparent for the frequency range of the RFID module [21, 22].

Two boards are located inside the sensor case: a signal processing module board and a transceiver board and the RFID tag. The signal processing module is installed at the bottom, above the terminals of the sensitive element, which is connected to the board using 4 wires. The purpose of this module is to convert the signal to a digital format and generate a message that complies with the RFID protocol. On the upper board, there is a transmitter and an RFID chip with a microstrip antenna, as well as batteries connected to it.

The MPCB of the signal processing module was analyzed in the course of the study. The conductive pattern occupied 4 layers in the initial version of tracing with the gaps for the vias. After re-wiring of the board using the Via-in-Pad method, the conductive pattern occupied only 2 layers. The method under study allowed increasing the tracing ability and improving the utilization of the space not only under the component but also around it. Consumer product features have been improved in accordance with safety requirements [23]. This made it possible to arrange the conductive pattern on two layers, thereby reducing the cost of the product.

Next, the Via-in-Pad method was analyzed for electrical properties: loss of resistance of the vias with a subsequent transition to the next layer [24]. For this purpose, formula (11) was used for the calculation of resistance, according to Russian GOST No. 55744-2013:

$$R=(pT)(3.14\cdot Dt), \qquad (11)$$

Where R is resistance, Ohm; t is the thickness of copper in the hole, mm; T is the thickness of the printed circuit board, mm; D is the diameter of the drilled hole, mm; p is the conductivity of copper. Copper conductivity of 100% is allowed.

The following characteristics are used for research: T = 2 mm, D = 0.2 mm.

The authors use pastes of the PCB-16, PCB-17, PCB-31, PPS-2 trademarks produced by JSC ELMA-PASTY. Silver pastes become increasingly popular as heat-conductive materials in blind via technology to improve heat removal from heat-sensitive components during soldering. These materials are often used as conductive ones in less important devices, where performance requirements do not imply the presence of well-metallized holes.

All pastes with low resistivity consist of silver and palladium in the ratio Ag/Pd: (10:0-10:1) and have a resistance of up to 750 μOhm. Since the resistances of metallization and paste are combined inside, these resistances are summed up as follows: R + R1, where the value of R1 takes into account an increase in the thickness of metallization and a decrease in the thickness of the paste (650-750 μOhm). Let the paste resistance be equal to the average value of –700 μOhm. When the paste dries, additional metallization is added on top of the paste and the contact pad, and together with the transition to the next layer, the MPCB is 15-20% of the resistance R. It should also be considered that the space required for the gaps between the vias and the contact pads is 50% of the additional metallization. Summing up, one can obtain $R=(pT)(3.14\cdot Dt)\cdot 1.2+R_1$ for the Via-in-Pad method, and $R=(pT)(3.14\cdot Dt)\cdot 1.3$ [25] for transition (Tabl. 1-2).

TABLE I
CALCULATION OF THE RESISTANCE OF THE METALLIZATION LAYER IN THE HOLE IN THE MPCB USING THE VIA-IN-PAD METHOD

Thickness of the copper in the hole t, μ	Total resistance R + R1, μOhm	The thickness of the copper in the hole t, μ	Total resistance R + R1, μOhm
9	713.6	54	781.4
18	727.1	63	794.9
27	740.5	72	808.5
36	754.2	81	822.1
45	767.8	90	835.6

TABLE II
CALCULATION OF THE RESISTANCE OF THE METALLIZATION LAYER IN THE HOLE IN MPCB WITHOUT FILLING

Thickness of the copper in the hole t, μ	Total resistance R, μOhm	Thickness of the copper in the hole t, μ	Total resistance R, μOhm
9	14.7	54	88.2
18	29.4	63	102.9
27	44.1	72	117.6
36	58.8	81	132.3
45	73.5	90	147

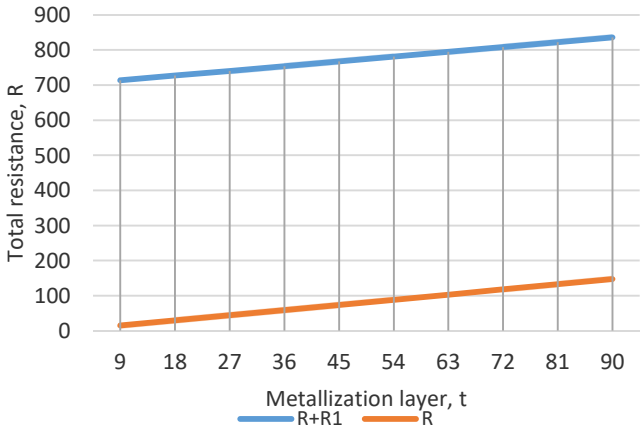


Fig. 8. Comparison of the resistance of the metallization layer in the hole in a 2-mm-thick MPCB without filling and formed by Via-in-Pad

Obviously, the holes with metallization without filling with conductive pastes have an internal resistance much lower than that of the holes formed using the Via-in-Pad method.

IV. CONCLUSION

The purpose of the proposed Via-in-Pad method is to solve the problem of space optimization by combining contact pads with vias. The obtained results confirmed the possibility of reduction of the usable space by 25%, which makes it possible to arrange more pads per unit area, to free up the gaps for BGA tracing, to reduce the pattern density and the path of critical signals and microwave signals, to reduce the time for drilling the workpieces, to reduce the

number of used drills, and also provides the best heat removal from the components. The disadvantage is the large internal resistance of the transitions created by the Via-in-Pad method, in contrast to the standard ones, which can negatively affect the flow of critical signals.

These results can be relevant for those design cases when it is necessary to fit a large number of components into small dimensions. In the future, it is planned to conduct further experimental studies to determine the dependence of the density of contact pads using the Via-in-Pad method, as a result of which it is planned to detect a quantitative decrease in the layers compared to conventional wiring.

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APPENDIX

LISTING OF THE EFFICIENCY EVALUATION ALGORITHM FOR THE VIA-IN-PAD METHOD

```
#include <iostream>
int Perex;
double Beta, Alfa, sCONMIN, h, H,sVIA, sPAD, l, g, dVIA, dPAD, sCONMAX,sZMIN, sZMAX, sZF, fMIN, fMAX, fZF,otn1, otn2, protn1, protn2, pi = 3.141592;

voidInputVar(){
cout « "Set the pad size" « endl « "Dpad = ";
cin » dPAD; // Pad size
cout « "Set the via size" « endl « "Dvia = ";
cin » dVIA; // Via size
cout « "Set the distance between pads" « endl « "g = ";
cin » g; //  Distance between pads
cout « "Set transition track thickness" « endl « "l = ";
cin » l; // Transition track thickness}

voidInputArithmetic(){
cout « "Set the pad size" « endl « "Dpad = ";
cin » dPAD; // Pad size
cout « "Set the distance between pads" « endl « "g = ";
cin » g; //  Distance between pads}

voidSomeArithmeticFor1(){
sPAD = (pi*pow(dPAD,2))/4; sVIA = (pi*pow(dVIA,2))/4; h = sqrt((3*pow(dVIA,2))/16);
H = sqrt((3*pow(dPAD,2))/16);Beta = 180 – 2*acos(l/dPAD)*(180/pi);
Alfa = 180 – 2*acos(l/dVIA)*(180/pi);}

voidSomeArithmeticFor2(){
sPAD = (pi*pow(dPAD,2))/4; // Contact pad area
sZF = pow(g, 2) – sPAD;
fZF = (1 – sZF / pow(g, 2)) * 100;}

int main() {
cout « "Enter 1 or 2" « endl;
cout « "1: with vias " « endl;cout « "2: without vias" « endl;cin » Perex;
switch (Perex){

case 1 :InputVar(); SomeArithmeticFor1(); sZF = pow(g, 2) – sPAD;fZF = (1 – sZF / pow(g, 2)) * 100; if (l <dVIA) {sCONMIN = l * (g * (sqrt(2)) / 2 – h – H) -((pow(dVIA, 2)) / 4) * (pi * Alfa / 180 – sin(Alfa * pi / 180)) -((pow(dPAD, 2)) / 4) * (pi * Beta / 180 – sin(Beta * pi / 180));
sZMIN = pow(g, 2) – (sPAD + sVIA + sCONMIN);fMIN = (1 – sZMIN / pow(g, 2)) * 100;otn1 = fMIN;}
else {sCONMAX = l * (g * (sqrt(2)) / 2 – H) -((pow(dVIA, 2)) / 4) * (pi * Beta / 180 -sin(Beta * pi / 180)) – sVIA / 2;sZMAX = pow(g, 2) – (sPAD + sVIA + sCONMAX);fMAX = (1 – sZMAX / pow(g, 2)) * 100;otn2 = fMAX;}
protn1 = otn1 – fZF;protn2 = otn2 – fZF;if (otn1 > 0) {cout « " The ratio of the occupied S in the zone of the contact pad to the S of the zone of the contact pad: " « protn1« " %" « endl;} else
cout « " The ratio of the occupied S in the zone of the contact pad to the S of the zone of the contact pad: " « protn2« " %" « endl;

case2 : InputArithmetic(); SomeArithmeticFor2(); cout « "1) The ratio of the occupied S in the zone of the contact pad to the S of the zone of the contact pad: " « sZF« " %" « endl; return 0;
default: cout «"Error, bad input, quitting\n";}
return 0;}
```